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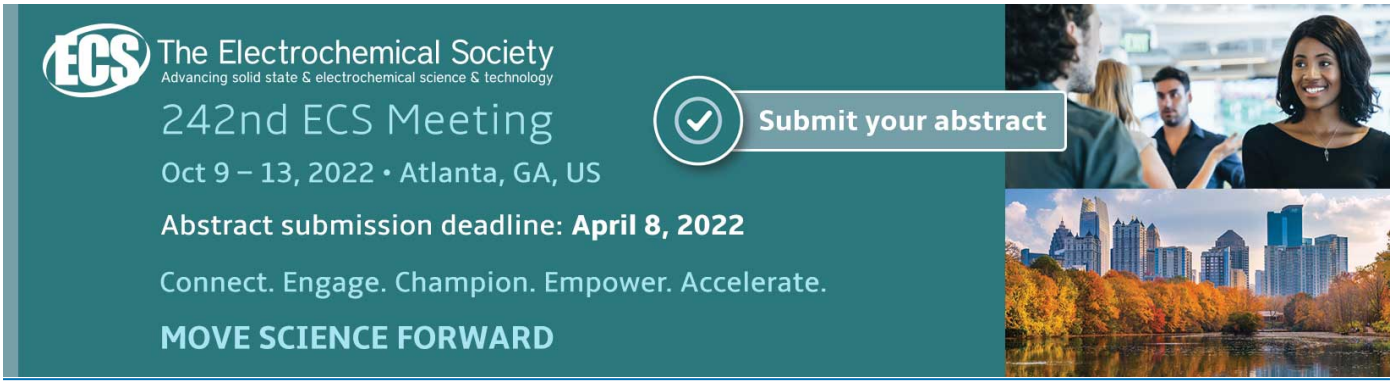

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Effect of the thermal stress on the defect evolution at GaAs/Si wafer bonding with a-Ge intermediate layer

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Abstract

In this paper, the bonding of GaAs wafer and Si wafer is achieved by introducing an amorphous Ge as the intermediate layer. Dislocations are observed on the GaAs surface when the GaAs/Si bonded wafers are annealed at 150 °C. The dislocation density is found to increase with the increase of the annealing temperature (from 150 °C to 350 °C). This feature can be explained by the increase of the thermal stress in the GaAs wafer due to the thermal mismatch between GaAs and Si wafers. With higher annealing temperature, such as 300 °C and 350 °C, some pits which originate from the partial cracking of GaAs surface are observed at the boundary of the bonded and unbonded regions. According to the stress simulation, the thermal stress at the bonding interface increases rapidly and reaches its maximum near the boundary of the bonded and unbonded regions, leading to the cracking of GaAs surface (formation of pits). In addition, large numbers of dislocations are generated near the pits. This may be attributed to the reduction of the nucleation energy of dislocations.

Supplementary material for this article is available online

Keywords: thermal stress, GaAs, Si, wafer bonding, defect

(Some figures may appear in colour only in the online journal)

1. Introduction

Compared with III–V semiconductors, silicon (Si) has the advantages of higher mechanical strength, higher thermal conductivity, and lower cost. Therefore, Si is regarded as an ideal supporting material for III–V semiconductors, such as GaAs on Si. However, due to the large difference of thermal expansion coefficients ($\alpha_{Si} = 2.6 \times 10^{-6}$, $\alpha_{GaAs} = 5.7 \times 10^{-6}$) and lattice constants ($\alpha_{Si} = 0.54$ nm, $\alpha_{GaAs} = 0.56$ nm) between these materials, high interfacial biaxial tensile stress ($\sim 10^8$ Pa) exists in the Si-based thin GaAs layer during epitaxial growth [1]. It is energetically favorable to be accommodated by a combination of elastic strain and interfacial misfit dislocation rather than by elastic strain alone with the increase of strained layer thickness [2–5]. The dislocations produced by the lattice mismatch acts as the acceptor-like defects at the middle of the bandgap, leading to the increase of the dark current of the photoelectric device. Although many modified GaAs/Si epitaxial methods were proposed to decrease the dislocation density, such as the two-step Ge intermediate layer growth [6], patterned Si growth [7], and GaAs buffer layer growth [8], The

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threading dislocation density of 10^6–10^7 cm^{-2} cannot be further reduced. More importantly, these growth methods were conducted at high temperature and for long time, leading to the increase of the cost [9–12].

Wafer bonding techniques, which are very different from the epitaxial growth techniques, have recently been applied to achieve the integration of Si and GaAs wafers [13–18]. These techniques can eliminate the stress caused by the lattice mismatch during epitaxial growth, while the thermal stress still needs to be addressed. Some low-temperature wafer bonding techniques also have been proposed to reduce the thermal stress in GaAs layer, for example, by employing polyimides, epoxies, spin-on-glasses, photoresist, and DVS-BCB, the wafer bonding can be performed at 120 °C or even lower temperature. However, due to the high resistance of these organic materials, these techniques are not suitable to fabricate photoelectric devices which are sensitive to the electrical conductivity at the bonded interface. Although O_2 plasma treatment and covalent direct bonding conducted at 400 °C can achieve carrier transport at the bonded interface [19–22], the thermal stress of GaAs/Si bonded wafers is as high as tens of MPa. This may lead to the deterioration of the performance of the optoelectronic devices. In order to reduce the thermal stress, the method in which a superlattice layer is introduced to control the stress were proposed [23]. However, the effect of thermal stress on the generation of dislocations at the bonded interface has hardly been studied so far.

In this paper, GaAs/Si bonded wafer was realized by introducing the amorphous Ge (a-Ge) intermediate layer [24, 25]. There are two advantages of wafer bonding by introducing a-Ge. One is that the introduction of a-Ge interlayer can prevent the host wafer from contacting handle wafer, leading to eliminating the stress caused by the lattice mismatch. In addition, the advantage of introducing a-Ge as the intermediate layer over polymer materials is that carriers can transport across the bonding interface, which make GaAs/Si heterojunction fabricated by inserting a-Ge maintain rectification characteristic. High bonding strength of >5 MPa is achieved for the GaAs/Si bonded wafers. Different annealing temperatures (150 °C–350 °C) are selected to study the effect of the temperature on the defect evolution in the bonded wafers. In addition, the finite element method is employed to calculate the thermal stress at GaAs/Si bonded interface.

2. Experiment

The 4 inch GaAs wafer (350 μm, etch pit density < 30, (100) 15° off toward <111>) and 4 inch (100)-ordered Si wafer (500 μm) were cut into 1 × 2 cm by dicing machine. The Si wafers were cleaned by the RCA method. For comparison, two series of GaAs wafers were cleaned by different methods (sample A and sample B). Sample A was ultrasonic cleaned by acetone, ethanol, and deionized water, respectively, for 10 min. Sample B was only ultrasonic cleaned by acetone and ethanol, respectively, for 10 min without deionized wafer. After that, both samples were immersed into the solution of HF: H_2O = 1:4 and the solution of isopropanol: HCl = 10:1 for 5 min. Finally, the rinse of deionized water was conducted.

After cleaning, the Si and GaAs were loaded into the magnetron sputtering chamber, and the sputtering of 10 nm thick a-Ge layer with the power of 120 W and the pressure of 0.5 Pa was conducted for 26 s when background vacuum of 1×10^{-4} Pa was achieved. Then, GaAs and Si were brought into contact by pressing for 60 s after taking out of the chamber. After that, the bonded GaAs/Si wafers were annealed at 150 °C, 200 °C, 300 °C, and 350 °C for 20 h, respectively, at a rate of 0.5 °C min^{-1} in the tube furnace under N_2 atmosphere.

In order to expose the GaAs bonding surface, the bonded wafers were immersed in a KOH aqueous solution (H_2O: KOH = 4:1) in a quartz beaker. The etching temperature of 80 °C was selected. After etching for 7–8 h, the Si handle wafers were totally etched away, reserving the bonding surface of GaAs for observation. Due to the fact that the etching of molten KOH occurs preferentially in the area where the strain is accumulated, the etch pits after etching were used to characterize the dislocations. Thus, GaAs was heated up to 400 °C in molten KOH for an hour to identify the dislocations.

The atomic force microscope (AFM) was used to reveal the surface morphology of the GaAs wafer before bonding. The ultrasonic scanning microscope (SAM-301) was used to characterize the unbonded region at the bonded interface. The universal testing machine (AGS-X 5KN) was used to test the bonding strength of the bonded wafers (1 × 1 cm). The scanning electron microscope (SEM) and optical microscope (OM) were used to reveal the etch pit of GaAs. The ANSYS software was applied to simulate the thermal stress at GaAs/Si bonded interface.

3. Results and discussion

Figure 1(a) shows the AFM images of GaAs surfaces with different cleaning methods. The root-mean-square (RMS) of 0.66 nm and 0.35 nm is achieved for sample A and sample B, respectively. This indicates that the RMS of GaAs increases for the sample cleaned with deionized water for 10 min. This can be explained by the fact that the Ga element is extremely unstable in the solution without high concentrations of hydroxyl ions [26]. The wafer bonding with a-Ge intermediate layer is a kind of hydrophilic bonding [27] and the RMS of the substrate is required to be below 0.5 nm [28]. Thus, the cleaning of GaAs wafer without deionized water is selected for further study.

The SAM images of the GaAs/Si bonded interface annealed at 150 °C, 200 °C, and 350 °C, respectively, are shown in figure 2. The white and black areas represent the unbonded and bonded region, respectively. Some unbonded areas were observed at the edge of the bonded wafer and lots of bubbles emerge at the bonded interface for the samples annealed at 150 °C and 200 °C. This can be explained by the fact that hydrogen, a by-product of hydrophilic reaction at the bonded

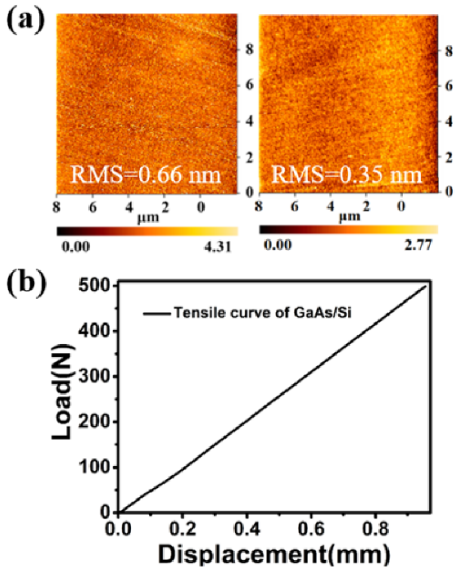

Figure 1. (a) AFM images of the surface of sample A (left) and B (right). (b) Tensile curve of the GaAs/Si bonded wafers annealed at 350 °C for 20 h.

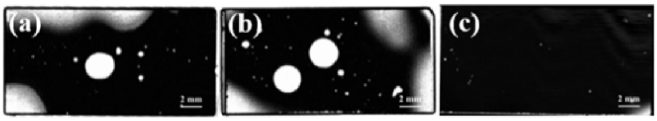

Figure 2. SAM images of the GaAs/Si bonded wafer. The bonded wafers annealed at (a) 150 °C, (b) 200 °C, and (c) 350 °C.

interface, hinders the perfect contact of the two substrates, leading to the separation of the contact surfaces. The reaction at the bonded interface can be given by equations (1) and (2). The reaction of hydroxyl groups attached to the surface forms the bridging oxygen bonds and water. The wafer diffuses into the surrounding native or thermal oxide to react with Si. Thus, the SiO_2 and hydrogen emerge at the bonded interface. On the other hand, the hydrogen is not completely eliminated due to the low-temperature annealing of the bonded samples, leading to the formation of unbonded regions (bubbles) at the interface. As shown in figure 1(b), the bonded wafer with the bonded area of 1 cm^2 is used for the tensile testing, the bonding strength of 5 MPa of the bonded wafers is obtained. This is enough for following machining process

$$Ge - OH + Ge - OH \rightarrow Ge - O - Ge + H_2O. \quad (1)$$

$$Si + 2HOH \rightarrow SiO_2 + 2H_2\,. \quad (2)$$

After selective etching of Si wafer with KOH solution, the bonding surface of GaAs is exposed. The GaAs surfaces are further etched by molten KOH to identify the dislocation pits, as shown in figure 3. The etch pits emerge on the bonding surface of GaAs in the sample annealed at 150 °C, as shown in

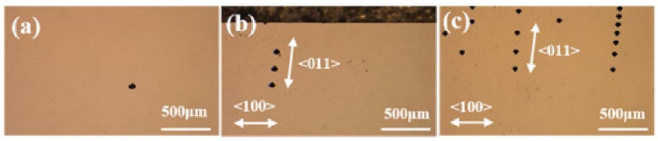

Figure 3. OM images of GaAs surface etched by molten KOH. The bonded wafers annealed at (a) 150 °C, (b) 200 °C, and (c) 350 °C.

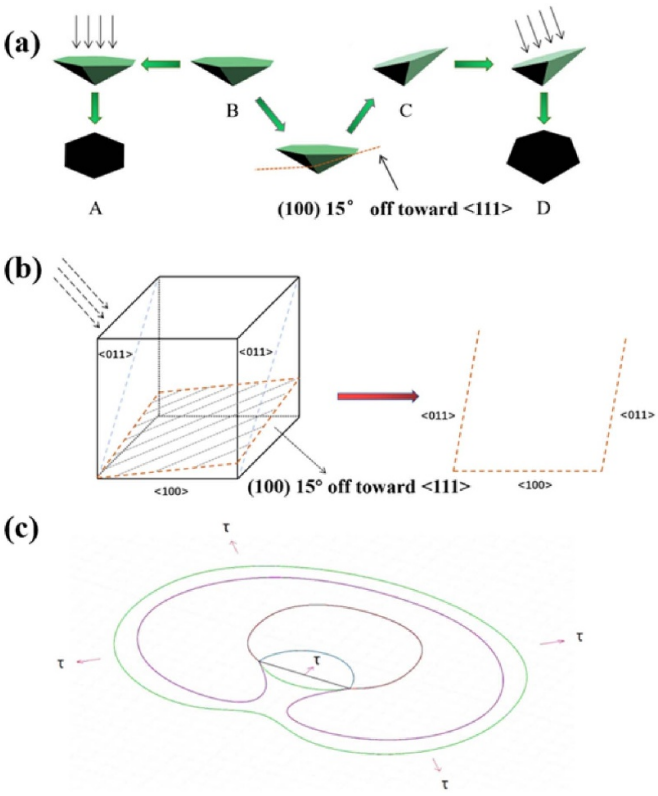

Figure 4. (a) The shape and front view of the etch pit on the surface of GaAs (100) 15° off toward <111> and GaAs (100). (b) Crystal orientation observed along the direction perpendicular to the plane (100) 15°off toward <111>. (c) The process of the Frank–Read multiplication mechanism.

figure 3(a). One can see that a sector-like etch pit is observed on the of GaAs surface. It was reported that the shape of the etch pits for the dislocations on the surface of GaAs (100) is a hexagonal pyramid, which is the same as B in figure 4(a). When the etch pit is observed along <100> direction, its shape is the same as A in figure 4(a). If the (100) plane is inclined by 15° along <111> direction (C in figure 4(a)), the shape of the etch pit becomes a hexagon that looks like a sector (D in figure 4(a)). This is the same as the shape of the pits observed in figure 3.

It can be concluded that the observed sector-like etch pits originate from the dislocations in the bonded GaAs wafer. This reveals that the thermal stress generated after annealing can indeed produce dislocations on the bonding surface.

Figures 3(b) and (c) show the etch pits on the GaAs bonding surface of the bonded wafer annealed at 200 °C and 350 °C, respectively. One can see that the etch pit density increases

with the increase of the annealing temperature. This may be due to the higher strain energy at higher annealing temperature induced by the difference of the coefficient of thermal expansion. Note that the etch pits are arranged along <011> direction, as shown in figure 4(b). The Frank–Read dislocation multiplication mechanism may be responsible for this feature. According to this theory, when the edge dislocation slips on the (111) crystal plane along the <011> crystal direction, it crosses with the pinning point (point defect) probably. This causes the two ends of the dislocation pinned by the nodes. However, due to the fact that the thermal stress in the direction perpendicular to the dislocation line drives the dislocation to slip along <011> direction and the dislocation line can only be bent due to two ends fixed. New dislocation loop is generated when the process in the figure 4(c) occurs. This process is endlessly cycle and produces a new dislocation loop every cycle to achieve dislocation multiplication. Thus, we believe that the increase of the etch pit density is attributed to dislocation multiplication. It can be seen that the dislocation is dense on the GaAs surface of the bonded wafer annealed at 200 °C and seriously denser on the surface of GaAs of the bonded wafer annealed at 350 °C. In order to further explain this feature, the finite element simulation is also conducted later.

The impurities may be leaved on the GaAs surface when the wafer is cleaned only by the organic and HF solution. This may hinder the contact of GaAs and Si during wafer bonding. Thus, some bonded wafers with unbonded regions were obtained. It can be observed that the shape of the etch pit on GaAs in the samples annealed at 300 °C and 350 °C with unbonded area is different from the shape of the etch pit on GaAs in the samples annealed at 350 °C without unbonded area. The SAM images of GaAs/Si bonded wafer annealed at 300 °C and 350 °C with some unbonded areas are showed in figures 5(a) and (b). The KOH solution is used to etch these bonded wafers and an original GaAs wafer in water bath at 80 °C for 8 h. After selective etching of Si wafer with KOH solution, a few pits are observed on the surface of GaAs. The pits appear in the area surrounded by red circle which is close to the unbonded edges in figures 5(a) and (b), as shown in figures 5(c) and (d). In addition, OM image of the original GaAs surface shows that no pit is observed in figure S1 (available online at stacks.iop.org/SST/36/095005/mmedia). Therefore, it can be inferred that the pits on the GaAs surface after etching of Si wafer are not caused by the etching of dislocations using KOH solution.

Figures 5(e) and (f) show the OM image of the surface in figures 5(c) and (d) further etched by molten KOH solution. A large number of strip-shaped etch pits form near the original pits. The areas marked by red circle in the figures 5(e) and (f) are the areas marked by red circle in figures 5(c) and (d). It also can be observed that the shapes of head and tail of the strip-shaped etch pits are similar to that of the single etch pit in figure 4.

In order to explain the formation of strip-shaped etch pits, the SEM images of the strip-shaped etch pits are shown in figure 6(a). One can see that each side of the strip-shaped etch pits are parallel to each other along a specific direction. This

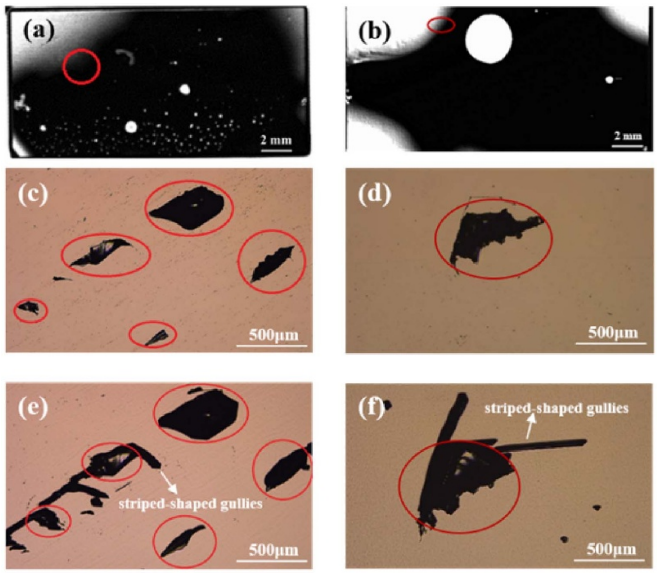

Figure 5. SAM images of GaAs/Si bonded wafers annealed at (a) 350 °C and (b) 300 °C. OM images of the GaAs surface in the samples annealed at (c) 350 °C and (d) 300 °C when Si wafer is etched. OM images of the GaAs surface in the samples annealed at (e) 350 °C and (f) 300 °C further etched by molten KOH.

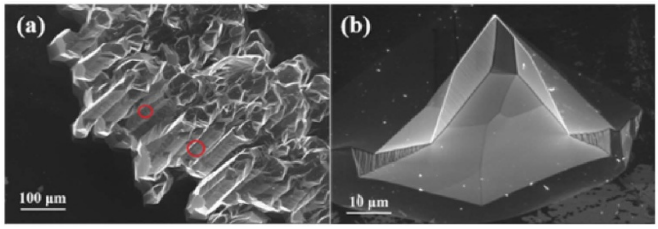

Figure 6. SEM image of (a) strip-shaped etch pits and (b) single etch pit on the GaAs surface in the sample annealed at 350 °C.

feature can be explained by the fact that etching of strip-shaped etch pits are along crystal orientation. This is consistent with the mechanism of the generation of the etch pits. In addition, the steps which look like the boundary of the etch pits are seen in the area surrounded by the red circles. The shape of the head of the strip-shaped etch pits is also same as the profile of the single etch pit, as shown in figure 6(b), as shown in figure S2. It can be concluded that the strip-shaped etch pits are derived from the connection of a large number of single etch pits.

Note that almost strip-shaped etch pits observed in figure 5 form near original pits due to the high thermal stress. It have been reported that when the dislocation nucleates near impurity or defects on the substrate surface, the dislocation nucleation energy decreases [29]. We believe that the defect near original pits lead to the nucleation of the dislocations. This requires less dislocation nucleation energy. Therefore, the dislocations may be formed preferentially near the pits. Dislocation nucleation with the above mechanism draw less energy from the elastic energy. Thus, lots of dislocations are

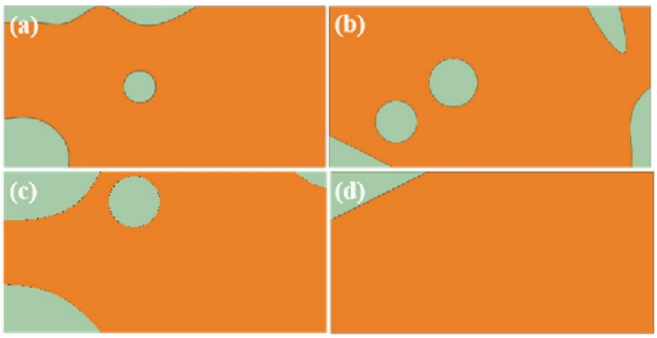

Figure 7. Images of the simulation model of the bonded wafer annealed at (a) 150 °C, (b) 200 °C, (c) 300 °C, and (d) 350 °C.

generated at the edge of the unbonded region to relax the strain energy compared with that in the bonded areas. Overall, the strip-shaped etch pits are due to the dense dislocations which are etched by molten KOH.

Note that the original pits are located at the boundary between the bonded and the unbonded regions. In addition, these pits are not observed for the bonded wafers annealed at 150 °C and 200 °C. This indicates that high thermal stress occurs at the boundary. In order to address this feature, a three-dimensional finite element simulation is performed to determine the distribution of the thermal stress at the bonded interface.

In the simulation, the Si wafer with thickness of 500 μm is defined as the host wafer and the GaAs wafer with thickness of 350 μm is defined as the handle wafer. Ten nanometer thick a-Ge is inserted between the two bonding wafers. Compared to direct bonding, the effect of the a-Ge layer on the thermal stress in GaAs can be ignored according to the simulating result, as shown in figure S3. Therefore, the a-Ge layer is not introduced in this simulation. Figure 7 shows the bonding interface definition. To depict the partially bonded GaAs/Si samples, the green areas stand for unbonded regions, and the orange areas stand for bonded regions. The shapes of the bonded areas are depicted according to SAM observations of the four samples in figures 2(a), (b) and 5(a), (b). The temperature is set to rise from room temperature to the annealing temperature. In addition, the thermal stress of the fully bonded wafer annealed at 150 °C, 200 °C, 300 °C and 350 °C are also calculated. The four vertices of Si are constrained in the z axis.

The material parameters listed in table 1 are used for this simulation. The mapping obtained indicates biaxial stress of GaAs at a distance of 1 μm from the bonding interface.

Figure 8(a) shows the thermal stress in fully bonded wafers annealed at 350 °C. One can see that the thermal stress in central region is homogeneous when all the areas are bonded. For the partially bonded sample, the thermal stress increases rapidly and it approaches maximum at the boundary between bonded and unbonded region, as shown in figures 8(b–e). The calculated thermal stress at the boundary and in the bonded region for the GaAs/Si bonded wafer annealed at 150 °C, 200 °C, 300 °C, and 350 °C is listed in table 2. One can see

Table 1. Material parameters for thermal stress simulation.

	Young's modulus (GPa)	Poisson's ratio	Thermal expansion coefficient (ppm K^1)	Density (g cm^3)
GaAs	85.9	0.31	5.7	5.37
Si	170	0.28	2.6	2.33

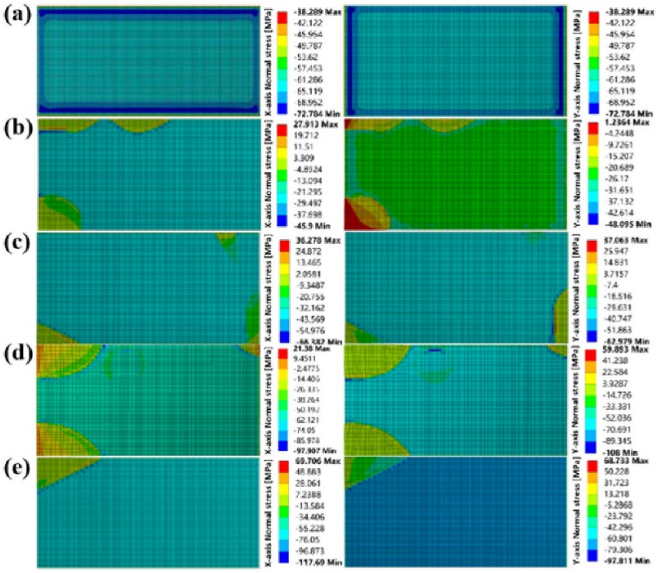

Figure 8. Mapping of the x- (left) and y- (right) stress of GaAs at a distance of 10 μm from the bonding interface. (a) The fully bonded wafer annealed at 350 °C, the partially bonded wafer annealed at (b) 150 °C, (c) 200 °C, (d) 300 °C, and (e) 350 °C.

that the thermal stress at the boundary is twice of that in the bonded region for bonded wafer annealed at 350 °C. When the annealing temperature drops to 300 °C, the stress at the boundary is still greater than the stress in the bonded region of the bonded wafers annealed at 350 °C. However, the thermal stress at the boundary for bonded wafer annealed at 150 °C and 200 °C is the same as that in the bonded region of the bonded wafer annealed at 350 °C, or even lower, leading to the absence of the pits. Overall, we assume that high thermal stress at the boundary for bonded wafer annealed at 300 °C and 350 °C may cause some microcracks on the bonding surface for extremely brittle GaAs, leading to the formation of the pits.

Table 2 shows that the thermal stress increases with the increase of the annealing temperature for the bonded region. On the other hand, the strain energy will increase as the thermal stress increases according to

$$U_{\mathrm{coh}} = h\sigma^{//}\varepsilon^{//}$$

where U_{coh} is the coherent energy, h is the thickness of the GaAs wafer, σ is the stress and ε is the strain. Therefore, more dislocations are formed to relax the strain energy. This is corresponding to the result of the experiment.

Table 2. Biaxial stress of GaAs at a distance of 10 μm from the bonding interface in the bonded area and at the boundary.

		Fully bonded sample		Partially bonded sample	
Temperature	Stress (MPa)	Center	Edge	Bonded area	Boundary (max)
150 °C	*x* direction	25	26	25	45
	y direction	25	26	25	37
200 °C	*x* direction	34	36	34	66
	y direction	34	36	35	62
300 °C	*x* direction	53	56	53	100
	y direction	53	56	56	81
350 °C	*x* direction	63	66	64	115
	y direction	63	66	64	96

4. Conclusion

In this article, the bonding of GaAs wafer and Si wafer is achieved by introducing amorphous Ge as the intermediate layer. The etch pits are observed on the GaAs bonding surface of GaAs/Si bonded wafer after annealed, indicating that the dislocations are formed due to thermal stress. The density of the dislocation on the surface of GaAs increases with the increase of the annealing temperature in the bonded area. The result of the simulation indicates dislocation increase due to higher strain energy caused by higher thermal stress. Some pits are observed near the boundary of the bonded and the unbonded area on the GaAs bonding surface of GaAs/Si bonded wafer annealed at 300 °C and 350 °C. According to calculated stress of the simulation, the thermal stress at the boundary of the bonded and unbonded area is greater than that in the bonded region, leading to the formation of the pits. In addition, a large number of the dislocations are generated near the pits. This may be attributed to reduction of the dislocation nucleation energy. In this paper, different kinds of defects are observed in the bonded area and the boundary between bonded region and unbonded region. By revealing the dependence of these defects and temperature, we trust that this work may provide guidance for the study on defects in the interface of devices based on the wafer bonding technique.

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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